

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 28

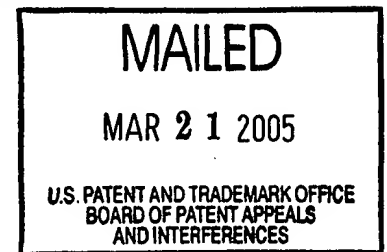
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY A. SHIELDS, TUAN D. PHAM,
MARK T. RAMSBEY, YU SUN,
ANGELA T. HUI and MARIA CHOW CHAN

Appeal No. 2004-2152
Application No. 09/728,554

HEARD: March 8, 2005¹



Before HAIRSTON, BARRETT, and LEVY, Administrative Patent Judges.
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1, 2, and 5-14. Claims 3 and 4 have been withdrawn from further consideration as a result of a restriction requirement (Paper No. 9, mailed May 16, 2002).

¹ Telephonic hearing.

BACKGROUND

Appellants' invention relates to a dual spacer process for non-volatile memory devices. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

1. A method for forming a spacer, comprising:

depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

applying a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area, the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Nakajima et al. (Nakajima)	5,329,482	Jul. 12, 1994
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Claims 1, 2, and 5-14 stand rejected under 35 U.S.C.
§ 102(e) as being anticipated by Nakajima.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejection,

we make reference to the examiner's answer (Paper No. 20, mailed August 18, 2003) for the examiner's complete reasoning in support of the rejection, and to appellants' brief (Paper No. 19, filed May 30, 2003) and reply brief (Paper No. 22, filed September 22, 2003) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR § 41.37(c)(1)(vii).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejection advanced by the examiner, and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

We observe at the outset appellants assertion (brief, page 3) that "[c]laims 1, 2, and 5-14 stand or fall together." In the

reply brief (page 3), appellants, through different counsel, repeat the assertion that claims 1, 2 and 5-14 stand or fall together. However, in the reply brief (pages 4 and 5), appellants additionally provide separate arguments for claims 5 and 9-12. Moreover, although appellants do not refer to claims 2 and 6 by number, the limitation of claims 2 and 6 has been argued in the reply brief (page 4). Under the rules that existed at the time appellants' reply brief was filed, the examiner did not have the right to file a supplemental answer to respond to appellants' newly presented arguments. "These arguments presented for the first time in the reply brief are untimely. Cf. Kaufman Company, Inc. v. Lantech, Inc., 807 F.2d 970, 973 n.*, 1 USPQ2d 1202, 1204 n.* (Fed. Cir. 1986); McBride v. Merrell Dow and Pharmaceuticals, Inc., 800 F.2d 1208, 1210-11 (D.C. 1986) ("We generally will not entertain arguments omitted from an appellant's opening brief and raised initially in his reply brief. . . . Considering an argument advanced for the first time in a reply brief, then, is not only unfair to an appellee, . . . but also entails the risk of an improvident or ill-advised opinion on the legal issues tendered.") See 37 CFR § 1.192(c)(5)." Although the examiner did not have an opportunity to respond to appellants' arguments, because under the rules that existed at the time of the reply

brief, the reply brief was not limited to newly presented arguments of the examiner in the answer. Accordingly, these newly-presented arguments will be considered, as we decline to remand the application to the examiner to respond to appellants' additional arguments since the teachings of Nakajima are clear.

From our review of all of the issues presented, we affirm-in-part. We begin with claim 1.

To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). As stated in In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) (quoting Hansgird v. Kemmer, 102 F.2d 212, 214, 40 USPQ 665, 667 (CCPA 1939))

(internal citations omitted):

Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient.

Thus, a prior art reference may anticipate when the claim limitation or limitations not expressly found in that reference are nonetheless inherent in it. See In re Oelrich, 666 F.2d at

581, 212 USPQ at 326; Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 630, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. See In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986).

Appellants assert (brief, page 4) that "[c]ontrary to the Examiner's assertions, Nakajima et al. fails to disclose, teach or suggest depositing a first oxide layer over at least *two adjacent polysilicon lines in each of a core area and a periphery area...implanting an area located between at least two adjacent polysilicon lines in the core area...the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines - as claimed in the subject application.*" It is argued (brief, page 5) that since Nakajima fails to teach adjacent polysilicon lines in the same area, that Nakajima necessarily fails to disclose doping of adjacent polysilicon lines in the same area. Appellants further assert (*id.*) that "[t]hus Nakajima et al.'s disclosure of *doping both sides of a single polysilicon line* is distinguishable and

different from doping *between* adjacent polysilicon lines in the same area in order to form sources and drains." In the reply brief, appellants assert that in Nakajima, two polysilicon lines are not disclosed for each of the core and periphery areas. Appellants add (reply brief, page 4) that even assuming that there are at least two polysilicon lines in each of the core area and the peripheral area, that Nakajima still does not meet the claim because the claim recites, in part, "at least two adjacent polysilicon lines in each of a core area and a periphery area" (underlining added).

The examiner's position (answer, page 3) is that Nakajima discloses at least two polysilicon lines 6 and 12 in each of a core area and a periphery area, and that (answer, page 4) Nakajima depicts only one transistor in each region for the sake of simplicity. The examiner adds that Nakajima refers to only one memory cell transistor repeatedly, also as an example, even though plural memory cells with their associated peripheral transistor are disclosed. We agree.

From our review of Nakajima, we find that Nakajima is directed to a method for producing a semiconductor memory device (col. 1, lines 13 and 14). Nakajima discloses that "[i]n a

semiconductor memory device, such as a dynamic RAM, a memory section consisting in a matrix array of a large number of memory cells and a peripheral circuit section . . . are formed one and the same substrate (col. 1, lines 28-33)." It is further disclosed that in a memory section, different layers are densely formed at an extremely small distance from each other (col. 1, lines 38-40). Nakajima further discloses peripheral circuit section P and memory cell section M (col. 2, lines 26 and 27). From the use of the term "section" we find reference to more than a single memory or peripheral cell or circuit. It is an object of the invention of Nakajima that part of the insulating film is not left between the peripheral circuit section and the memory cell section (col. 2, lines 57-61). Further, from the disclosure of Nakajima that the source regions and the drain regions of MOS transistors of the memory cell section and the peripheral circuit section consist in high concentration impurity regions, (col. 2, lines 64-68), and that each of the MOS transistors has a sidewall formed on a lateral side of a gate electrode (col. 3, lines 1-4), we find further evidence that Nakajima is referring to plural transistors in each of the memory cell section M and the peripheral circuit section P.

From these teachings of Nakajima, we are unpersuaded by appellants' argument that Nakajima's reference to a memory cell and peripheral transistors does not refer to plural adjacent transistors in each of the memory cell and peripheral circuit areas. We are not persuaded by appellants assertion that even if Nakajima discloses plural transistors that there is no disclosure that they are adjacent to another transistor in the area or region. From the disclosure that in semiconductor memory devices, a memory section consists of a matrix array of a large number of memory cells and a peripheral circuit section (col. 1, lines 28-33) we find that an artisan would understand the disclosure of Nakajima to refer to plural adjacent cells in the memory section and the peripheral section, and would not understand the reference to refer to a single memory cell transistor and a single peripheral circuit transistor in each of the memory cell section and the peripheral circuit section, as asserted by appellants. To establish anticipation, the reference must disclose, explicitly or under the principles of inherency, the claimed invention. We are cognizant that inherency cannot be established by possibilities or probabilities, but must necessarily flow from the disclosure of the reference. We find this to be the situation here, where Nakajima inherently

discloses plural adjacent polysilicon lines in each of the memory (core) and peripheral areas. However, claim 1 requires more. The claim additionally requires that "the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines." From our review of Nakajima, we fail to find this limitation, and note that the examiner has not pointed to any portion of Nakajima that discloses this limitation, despite the fact that appellants argue (brief, page 4) that this limitation is not taught by Nakajima. Accordingly, we find that Nakajima fails to teach all of the limitations of claim 1. The rejection of claim 1 under 35 U.S.C. § 102(e) as being anticipated by Nakajima is therefore reversed. As claim 2 depends from claim 1, the rejection of claim 2 is also reversed.

We turn next to independent claims 5 and 13. At the outset, we make reference to our findings, supra, with respect to the teachings of Nakajima as they relate to claim 1. We note that unlike claim 1, independent claims 5 and 13 do not recite "the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines" as recited in claim 1. From the language of claims 5 and 13, we

find that because Nakajima discloses at least two adjacent polysilicon lines in each of a core area and a periphery area, the rejection of claims 5 and 13 under 35 U.S.C. § 103(a) is affirmed.

We turn next to claim 6. The examiner's position (answer, page 3) that "Nakajima et al also teaches that the first oxide layer has a thickness of less than one-half the distance between a periphery of the adjacent polysilicon lines (Figure 5)."

Appellants assert that Nakajima does not disclose any distances between adjacent polysilicon lines in the same area, because the drawings are not to scale and no reasonable distances/measurements can be construed therefrom.

From our review of Nakajima, we agree with appellants that Nakajima's drawings are not to scale, and that the examiner cannot rely upon figure 5 for a teaching that the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines. Accordingly, we find that the examiner has failed to establish a prima facie case of anticipation of claim 6. Accordingly, the rejection of claim 6 under 35 U.S.C. § 102(e) is reversed.

We turn next to claims 7 and 8, which depend from claim 5. We will sustain the rejection of claims 7 and 8, for the reasons set forth in the answer and the disclosure of Nakajima (figure 11) showing a second spacer etch, and the disclosure (figure 9) of implanting an area after the first spacer etch (figure 8). From these teachings of Nakajima, and the facts that claims 7 and 8 have not been separately argued, and appellants assert (reply brief, page 4) that their patentability depends from their dependence from claim 5, the rejection of claims 7 and 8 under 35 U.S.C. § 102(e) is affirmed.

We turn next to claims 9 and 10. We will sustain the rejection of claims 9 and 10 from the disclosure of Nakajima (figure 9) of implanting the periphery area, and the disclosure of Nakajima that the implanting is done after the first spacer etch (figure 8). Accordingly, the rejection of claims 9 and 10 under 35 U.S.C. § 102(e) is affirmed.

We turn next to claims 11 and 12. We will sustain the rejection of claims 11 and 12 from the disclosure of Nakajima (figure 12) of implanting an area between at least two polysilicon lines in the core (memory cell section) after the performing of the second spacer etch (claim 11), and our findings as to the disclosure of Nakajima with respect to claim 5, from

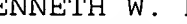
which claim 12 refers. Accordingly, the rejection of claims 11 and 12 under 35 U.S.C. § 102(e) is affirmed.

We turn next to claim 14. We will sustain the rejection of claim 14 in view of the disclosure of Nakajima (figure 12) of implanting an area located between at least two polysilicon lines in the core (memory cell section) area, and because appellants have not argued the limitations of claim 14, but rather let claim 14 fall with claim 13, from which claim 14 depends (brief, page 3).

CONCLUSION

To summarize, the decision of the examiner to reject claims 1, 2 and 6 under 35 U.S.C. § 102(e) is reversed. The decision of the examiner to reject claims 5 and 7-14 under 35 U.S.C. § 102(e) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136 (a)(1)(iv) (effective September 13, 2004; Fed. Reg. 49960 (August 12, 2004); 1286 Off. Gaz. Pat. and TM Office 21 (September 7, 2004)).


KENNETH W. HAIRSTON
Administrative Patent Judge


LEE E. BARRETT
Administrative Patent Judge


STUART S. LEVY
Administrative Patent Judge

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